IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael Andrew Fischer

Title: PARTIAL QUEUING USING AN INTERFACE WITH BOUNDED LATENCY

Appl. No.:   10/611,304

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Examiner: Mon Cheri S. Davenport

Art Unit: 2462

Confirmation   5599
Number:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

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Sir:

In accordance with the **Pre-Appeal Brief Conference Pilot Program**, announced July 11, 2005, this Pre-Appeal Brief Request is being filed together with a Notice of Appeal and the required Notice of Appeal fee. This communication is responsive to the Final Office Action dated September 14, 2010, concerning the above-referenced patent application. Accordingly, this pre-appeal brief is timely filed.

I.   The Examiner provides no support for the anticipation rejection of Independent Claims 30, 39, and 47

"In every Office action, each pending claim should be mentioned by number, and its treatment or status given." MPEP § 707.07(i). On page 2 of the Final Office Action, the Examiner asserts that Claims 30, 39, and 47 are allegedly anticipated by U.S. Patent No. 6,813,266 (Chiang). The Examiner, however, fails to provide any "treatment" of Claims 30, 39, and 47. As noted in the Office Action Response dated July 6, 2010, the Examiner failed to provide any support for the conclusion that Claims 30, 39, and 47 are anticipated by

Chiang in the previous Non-Final Office Action. In the Final Office Action, the Examiner has again failed to provide any support for the conclusion that Chiang anticipates Claims 30, 39, and 47. Accordingly, Applicant respectfully submits that the rejection of Claims 30, 39, and 47 is improper and should be withdrawn.

II. Chiang does not disclose the claimed "initiating a transmission of the first point of the first frame into a shared communication channel."

Claim 30 recites in part: "initiating a transmission of the first portion of the first frame into a shared communication channel." Claims 39 and 47, although of different scope, recite similar elements. In Section 2 of the Final Office Action, the Examiner asserts that Claims 30, 39, and 47 are anticipated by Chiang. The Examiner, however, does not provide any support for this assertion in Section 2. In the Response to Arguments section, the Examiner asserts that "Chiang teaches the outputs the forwarding descriptor including the port vector and the frame pointer into a port vector FIFO, which is the initiation process, which contains a portion of the frame data, less then full frame length." Later on page 13, The Examiner asserts that the claimed "first portion" is analogous to the port vector disclosed in Chiang. Applicant respectfully disagrees.

The port vector cannot be a "first portion of the first frame," as the port vector is never transmitted "into a shared communication channel." The port vector identifies "each MAC port that should transmit the data frame." Col. 5, lines 54-55. "The port vector has a bit set for each output port to which the frame should be forwarded." Col. 7, lines 35-36. "The port vector is examined by the port vector FIFO 56 to determine which particular output queue should receive the associated frame pointer." Col. 7, lines 43-45. Thus, Chiang teaches that a port vector identifies the various output ports/queues that should receive a particular frame pointer. Applicant submits that a port vector, therefore, cannot be the claimed "first portion of the first frame" transmitted "into a shared communication channel."

Additionally, Applicant submits that Chiang teaches only transmitting an entire frame from a single buffer and therefore does not disclose the claimed "initiating a **transmission of the first portion** of the first frame into a shared communication channel." (Emphasis added). Chiang is generally directed toward a network switch. *See* Abstract. The switch "includes a

media access control (MAC) module 20 that transmits and receives data packets to and from 10/100 Mb/s physical layer (PHY) transceivers 16 [and] a gigabit PHY." Col. 3, lines 37-45. "The MAC unit 20 obtains a free buffer location (*i.e.*, a frame pointer) from the free buffer queue 64, and outputs the received data packet..." Col. 5, lines 19-21. Thus, Chiang teaches that the entire data frame is stored in the free buffer queue, and that a frame pointer points to the location of a received data frame.

An "internal decision making engine 40, referred to as an internal rules checker (IRC), makes from forwarding decisions for data packets received." Col. 5, lines 1-3. The "internal rules checker 40 outputs a forwarding decision to the switch subsystem 42 in the form of a forwarding descriptor[, which] includes ... a port vector [and the] frame pointer." Col. 5, lines 50-58. The "port vector FIFO 56 decodes the forwarding descriptor including the port vector, and supplies the frame pointer to the appropriate output queues." Col. 5, lines 62-65. Using the port vector, "the port vector FIFO 56 places the frame pointer into the top of the appropriate quest 58 and/or 68. This queues the transmission **of the frame**." Col. 7, lines 45-48. (Emphasis added). "At some point in time, the frame pointer reaches the bottom of an output queue 58..." Col. 7, lines 59-60. "The dequeuing logic 76 for the transmit gigabit port 24*b* takes the frame pointer from the corresponding gigabit port output queue 58*d*, and issues a request to the scheduler 80 **to read the frame data** from the external memory 36...." Col. 7, lines 62-65. (Emphasis added). "[T]he dequeuing logic 76 reads the frame data (along the read bus 69*b*) in a DMA transaction ... and stores the frame data in the internal transmit FIFO...." Col. 8, lines 2-6. The frame pointer is used to write "the **entire frame data into the transmit FIFO**." Col. 8, lines 9-10 (Emphasis added). Thus, Chiang teaches writing all of the frame data into a transmit queue for transmission. Applicant submits that this is clearly not "initiating a transmission of **the first portion of the first frame** into a shared communication channel." (Emphasis added).

Accordingly, for at least the reasons above, Applicant respectfully requests the withdrawal of the rejection from the pending claims.

III.   Chiang does not disclose the claimed "receiving, at a lower medium access control entity, a first portion of a first frame, wherein the first portion is less than a frame length; ... responsive to initiating the transmission, receiving at the lower medium access control entity a second portion of the first frame."

Claim 30 recites in part: "receiving, at a lower medium access control entity, a first portion of a first frame, wherein the first portion is less than a frame length; ... responsive to initiating the transmission, receiving at the lower medium access control entity a second portion of the first frame." Claims 39 and 47, although of different scope, recite similar elements. In Section 2 of the Final Office Action, the Examiner asserts that Claims 30, 39, and 47 are anticipated by Chiang. The Examiner, however, does not provide any support for this assertion in Section 2. In the Response to Arguments section on page 8, the Examiner asserts that the claimed "first portion" is analogous to the port vector disclosed in Chiang and the "second portion" is the "data frame remainder." Applicant respectfully disagrees.

First, Applicant submits that Chiang does not disclose a "data frame remainder" anywhere in its specification. Accordingly, Applicant is unsure which feature of Chiang is being asserted. Not withstanding this deficiency, Applicant submits that based upon the Examiner's assertion that the "port vector" is the "first portion of a first frame," Chiang cannot disclose a "lower medium access control entity" that receives both "a first portion of a first frame" and "a second portion of the first frame."
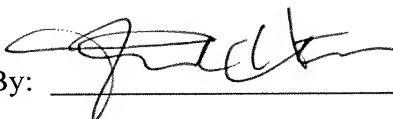
As noted above, the Examiner asserts that the port vector is analogous to the claimed "first portion of a first frame." The "rules checker 40 outputs the forwarding descriptor including the port vector and the frame pointer into the port vector FIFO 56." Col. 7, lines 41-43. Thus, Chiang teaches that the port vector FIFO receives the forwarding descriptor, which includes the port vector. As the Examiner asserts that the port vector is the "first portion of a first frame," the port vector FIFO, therefore, must be asserted as being analogous to the claimed "lower medium access control entity." Chiang, however, does not disclose that that the port vector FIFO receives any data other than the forwarding descriptor. Thus, Chiang teaches a port vector FIFO that receives only a port forwarding descriptor. Accordingly, Chiang cannot teach a "lower medium access control entity" that receives both "**a first portion of a first frame**" and "**responsive to initiating the transmission** [of the first

portion of the first frame], ... **a second portion of the first frame**." (Emphasis added). Accordingly, for at least the reasons above, Applicant respectfully requests the withdrawal of the rejection from the pending claims.

Respectfully submitted,

Date:_____November 3, 2010_____   By: _____

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